REMARKS

Claims 1-17 and 19-32, of which claims 1, 14 and 27 are independent claims, are currently pending in the application. Claims 1-2, 4-10 are rejected under 35 U.S.C. 102(b) as anticipated by U.S. 5,446,529 to Stettner et al. Claims 3, 10-17 and 19-32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Stettner in view of U.S. 5,015,868 to Park. Applicants traverse the rejections.

Claim 1 recites "a switchable current source that can be turned on or off, which when on provides *a predetermined current* that flows into the integrator". Stettner does not comprise a switchable current source that provides *a predetermined current* that is integrated by an integrator (*i.e.* storage capacitors 25 in Stettner's circuit 19, see Fig. 5 and column 6 lines 31-40). Current provided to Stettner's capacitors is current generated responsive to "return signals measured in 10's or 100's of photons" by "a photon signal amplifier with enough gain to amplify the signal above receiver noise" (column 9 lines 27-32). As a result, current integrated by Stettner is variable and a function of the number of photons in the return signals that reach Stettner's receiver.

Claim 1 further recites circuitry that turns the switchable current source on or off responsive to a signal generated by a photosensor. Stettner's circuitry does not comprise a controller that turns any current source on or off responsive to a signal generated by a photosensor. Stettner does not gate current; Stettner instead gates integrators, *i.e.* the various capacitors that Stettner's circuitry contains.

In view of the above Stettner does not support a prima facie anticipation rejection of claim 1.

Applicants traverse the 35 U.S.C. 102(b) rejection of dependent claim 5 and submit that the limitation recited by claim 5, that the circuit is formed as a monolithic integrated circuit, is not anticipated by Stettner.

There is nothing in Stettner that teaches a monolithic integrated circuit comprising all the components recited in claim 1 from which claim 5 depends. All of Stettner's circuits comprise an array of unit cells 10 each having analog electronics 19 formed *on a chip unit 7*. As noted by the applicants in the response filed on September 16, 2005, none of unit cells 10 comprises a light sensitive element that provides current to the cell electronics responsive to light. The light sensitive elements for each cell 10 are provided either by a photocathode 82 on an entrance window 8 that is not physically connected to the chip unit 7 (col 5 lines 59-60, Figs. 2-4) or by photodiodes 41 formed on a *separate diode array chip 40* (column 7 lines 36

and 37) each of which is connected to a different unit cell 10 by an indium bump 42 (column 7 lines 33- 50 and Fig. 9) on chip unit 7.

Whereas the Examiner contends that the configuration of chip unit 7 (having units 10) and diode array chip 40 (having photodiodes 41) connected by indium bumps can be considered as providing "an electronic circuit ... formed on or in said semiconductor surface (e.g. the photodiode array 41 and unit cells 10 are integrated in and formed on the semiconductor surface 7 of the image sensor 3)" there is no way either of the Stettner configurations can be construed to be a monolithic integrated circuit. The Stettner reference itself refers to the indium bump configuration as a "hybrid" (column 7 line 36, see also column 6 line 24) - *the antithesis of a monolithic integrated circuit.*

With respect to claim 5 under 35 U.S.C. 102(b), the Examiner contends that "the Stettner reference discloses wherein the circuit is formed as a monolithic integrated circuit (CMOS image processing chip 7)". Applicants submit that it is irrelevant whether or not chip 7 and its circuits are considered to be formed as a monolithic integrated circuit - chip 7 does not comprise the photosensitive elements claimed in claim 1 and therefore cannot be considered to anticipate claim 5. The Examiner's own rejection of claim 1 and response to the applicants arguments filed on September 16, 2005 attest that the circuits on processing chip 7 do not have light sensitive elements and that the light sensitive elements are provided by chip unit cell 10 connected to chip 7 by indium bumps, *which configuration is considered by Stettner to be a hybrid circuit.*

With respect to independent clam 14, neither Stettner nor Park in any manner teach, describe, or hint at, a semiconductor surface comprising pixels that have a circuit comprising a photosensor, a switch and an output terminal, and *that provides a signal on the output terminal only while light is incident on the photosensor and the switch is closed.* None of the light sensitive circuits in Stettner or Park produce signals only while light is incident on them. In general they produce signals at some time after they are exposed to light. Stettner's integrators provide output signals once they are charged after exposure to light and as noted on column 8 lines 50-53, "The three-dimensional image data is read off the array and digitized *during the relatively large time between laser pulses* (typically a few milliseconds)" (italics added), *i.e.* when light is not incident on the array. Park's light sensitive circuit is a CCD (see, *e.g.* Abstract) which of course stores an image and produces signals long after light that generates the image is no longer present. The combination of Stettner and Park cannot and does not provide the invention claimed in claim 14 and therefore does not support the prima facie

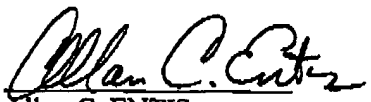
rejection promulgated by the Examiner. Claim 14 must therefore be considered patentable over the cited references.

Claim 27 is a method claim corresponding to claim 14 and is patentable over Stettner and Park at least for the same reasons that claim 14 is patentable over the references.

Dependent claims in the claim set that are not specifically referred to in these Remarks are patentable either through their dependence on independent claim 1, 14 or 27 and/or because of patentable material that they contain.

In view of the above, applicants submit that all the pending claims are patentable and that the application is in condition for allowance. Applicants respectfully request that the Examiner retract the finality of the present office action, review the Remarks and allow the application. If the Examiner does not agree regarding one or more of the claims, but is of the opinion that a telephone conversation may forward the present application toward allowance, applicants respectfully request that the Examiner call the undersigned at 1 (877) 428-5468. Please note that this is a direct *toll free* number in the US that is answered in the undersigned's Israel office. Israel is 7 hours ahead of Washington.

Respectfully submitted,
Ori J. BRAUN, et al.



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